CMOS Interconnects Beyond 10 GHz

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The continuous scaling of CMOS transistors has enabled more than a ten-fold increase in processor speed per decade. The demonstrations of transistors with less than 0.1µm gate lengths and higher than 100 GHz f_T indicate that there are no fundamental limits to this trend for the next decade. However, I/O speed is generally not keeping up with the core frequency, and the clock distribution and global interconnects on the chip have delays exceeding several gate delays. CMOS on-chip interconnects and I/O's are therefore considered potential bottlenecks to Moore's law. In our study, interconnects for both high-speed analog and digital applications were investigated.

In digital circuits, the existence of several metal layers without a reference ground plane results in uncertain return paths for high-speed clocks and buses. The parasitic inductance could cause unwanted clock skew and ringing. As the technology scales, progressively shorter interconnects will be dominated by inductive effects, causing a design challenge for large digital circuits. A five-layer 0.25µm test chip with a power grid and random lines was designed to characterize the inductance of realistic on-chip interconnects. A new inductance-sensitive ring oscillator was also implemented.

In analog circuits, products above 10 GHz are currently only available in III-V technologies such as GaAs. It is generally believed that the losses in the metal lines, the dielectric and the silicon substrate of a CMOS integrated circuit are the major limitations of operation above 5 GHz. However, by reducing the coupling to the substrate and using coplanar wave guides that take advantage of the reverse scaling of the top metal layers, transmission lines with a loss of 0.3dB/mm were achieved at 50 GHz. *Ku*-band amplifiers and oscillators were also implemented. To date, they are the only conventional CMOS circuits to achieve higher than 10 GHz operating frequencies.